

Modelling and Simulation with Spice of Power VDMOSFET Transistor

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Abstract- This paper provides a behavioral model in Pspice for a power MOSFET rated at 60V / 80 A for a wide temperature range. The Pspice model was built using device parameters extracted through experiment. The static and dynamic behavior of the power MOSFET is simulated and compared to the measured data to show the accuracy of the Pspice model. The temperature dependent behavior was simulated and analyzed.

Keywords- MOSFET device; Power VDMOSFET; Power semi-conductors devices; Thermal design; Spice; Device modelling.

I. INTRODUCTION

Circuit simulators play an important role in the development of modern electronic systems. Pspice is one of these simulators. When it comes to power devices it fails to simulate the inherent self-heating effect of the device where Power dissipation results in a rise in junction temperature. To overcome this, we developed a model that can adjust temperature dependent parameters.

The MOSFET model reference on which this work is based has been explained in [1]-[2]-[3]. The reader is encouraged to refer to these references for a full understanding of the MOSFET model parameters herein referred to as the standard SPICE MOSFET model. Recent works [8]-[9] have demonstrated methods of circumventing the SPICE global temperature definition, providing a means of using the device's own junction temperature as a self-heating feedback mechanism.

The model developed in [8] has limitations involving proprietary algorithms, rendering the method of limited interest. Model implementation is convoluted, involving an analog behavioural MOSFET model (ABM) whose operating characteristics are dependent on a SPICE level-3 NMOS MOSFET. As a result, both the switching circuit and the load must be duplicated for the model to function. The implementation in [9] does not model the drain-source

avalanche property of a MOSFET. Neither [8] nor [9] attempt to model the temperature characteristics of the intrinsic body diode.

I. STANDARD SPICE MOSFET MODEL

The macro-model in Figure 1 is that used in many Fairchild MOSFET device models. It is the evolution of many years of work and improvements from numerous contributors [1]-[7]. A significant advantage of this model is that extensive knowledge of device physics or process details are not required for implementing parametric data within the model. The following data curves are the basis used to generate the macro-model over temperature: transfer characteristic, saturation characteristic, $R_{ds(on)}$, gate threshold voltage, drain-to-source breakdown voltage, intrinsic body diode voltage, capacitance versus drain-to-source voltage, and gate charge waveform. Parametric data for up to five temperature points are used for model calibration resulting in a macro-model that provides representative simulation data for any rated operating junction temperature. The limitation of the standard MOSFET model is found in simulations involving severe pulsed power dissipation, and parallel operation. Reliance of the SPICE MOSFET primitive on the global analysis temperature variable (.TEMP SPICE instruction) results in simulations having all MOSFETs operating at a single predefined temperature. Device behaviour under high power dissipation transitory excursions cannot be accurately modeled. Threshold voltage and $R_{ds(on)}$ are but two of the important parameters that can change sufficiently as to render a simulation inaccurate

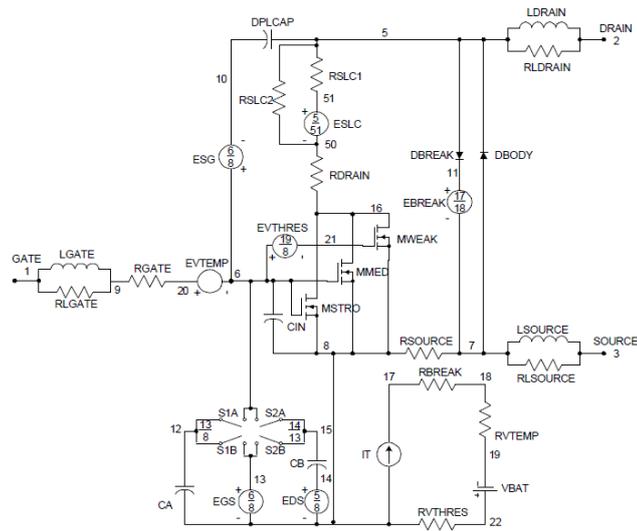


Figure.1 Standard MOSFET Macro-model Dependent on Global Temperature Definition

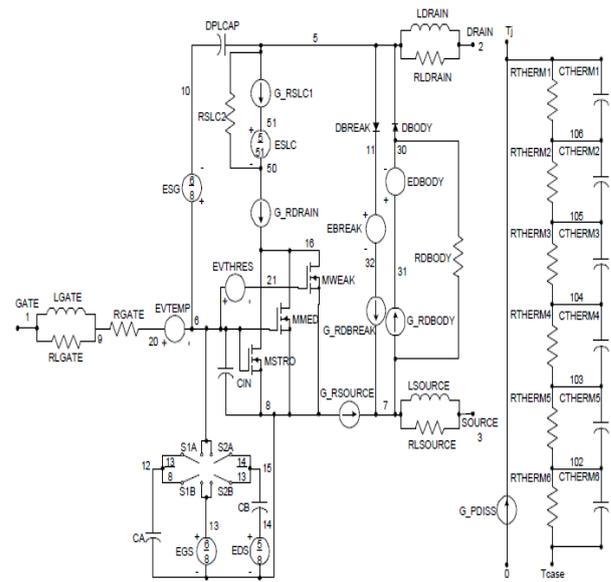


Figure.2 Self-Heating MOSFET Macro-model Independent of Global Temperature Definition

I. SELF-HEATING SPICE MOSFET MODEL

Improved implementation of static and dynamic behaviour is achieved with the self-heating SPICE MOSFET model (Figure 2), an evolution of the standard MOSFET model (Figure 1). Improved implementation of static and dynamic behaviour is achieved. Temperature dependent model parameters respond in closed loop form to the junction temperature information provided by node Tj. Performance is independent of SPICE's global temperature definition .TEMP, circumventing the level-1 NMOS model primitive self-heating limitation. All MOSFET operating losses are inclusive in the current source G_Pdiss (scaling of 1A = 1W dissipation) representing instantaneous power dissipation into the thermal model.

Multiple MOSFETs may be simulated at different and variable junction temperatures. Each MOSFET can be connected to a heat sink model via node Tcase. The heat sink model can be device specific, so heat sink optimization becomes possible. Current source G_Pdiss is referenced to the simulation ground reference, permitting use of the model in bridge topologies

It may be used as a monitoring point, or it may be connected to a defined voltage source to override the self-heating feature. Tcase must be connected to a heat sink model. Treatment of connections to the model's gate, drain, and source terminals are no different than those of the standard MOSFET model.

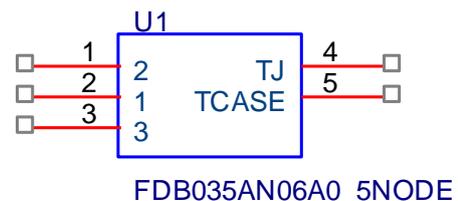


Figure.3 Self-Heating Power MOSFET PSPICE Symbol

II. SELF-HEATING MODEL IMPLEMENTATION

Ability to describe the value of a resistor and its temperature coefficients as a behavioural model referenced to a voltage node is necessary to express dependence on junction temperature. SPICE resistor ABMs do not permit voltage node references. Dynamic temperature dependence of the MOSFET's resistive element (expressed as separate lumped elements) and of the diode's resistive component cannot be implemented without a resistor behavioural model. This limitation is overcome by using a voltage controlled current source ABM expression (Figure 4). By using the nodes of the current source for voltage control, it becomes possible to express a resistor as a voltage-controlled current source by implementing the expression for the resistor's current as $I = V/R(T_j)$. The resistance $R(T_j)$ becomes a behavioural model expression dependent on the voltage node Tj representation of junction temperature. This voltage-controlled current source ABM

model was used to modify the standard MOSFET model from Figure 1 by implementing voltage dependent versions of RDRAIN, RSOURCE, and RSLC1. Behavioural expressions were implemented in the self-heating model to eliminate IT, RBREAK, RVTEMP, and VBAT through modification of EVTEMP, EVTHRES, and EBREAK.

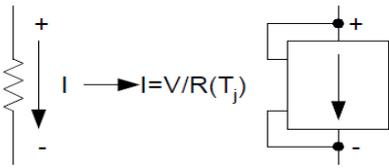


Figure.4 Implementing a Voltage Dependent ABM Resistor Model

Temperature dependent resistive elements of diodes DBODY and DBREAK were separated from the diode model and expressed as voltage controlled current source ABM models G_RDBODY and G_RDBREAK. A large value resistor RDBODY was added to improve convergence. EDBODY is added in series with DBODY to incorporate the intrinsic body diode forward conduction drop temperature dependency. Junction temperature information is implemented by the inclusion of the thermal network Z_{0JC} and current source G_P_{DISS}. The thermal network parameters are supplied in Fairchild data sheets. G_P_{DISS} calculates the MOSFET instantaneous operating loss, and expresses the result in the form of a current using the scaling ratio of 1A=1W. This is a circuit form implementation of the junction temperature from expression (1)

$$T_J = P_{Dissipation} \cdot Z_{0JC} + T_{case} \quad (1)$$

Where T_J = junction temperature, P_{Dissipation} = instantaneous power loss, Z_{0JC} = thermal impedance junction-to-case and T_{case} = Case temperature. T_J and T_{case} use the scaling factor 1V = 1°C.

III. STATIC CHARACTERISTICS SIMULATION

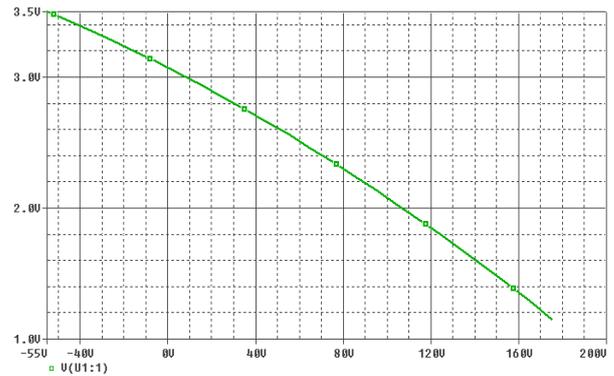
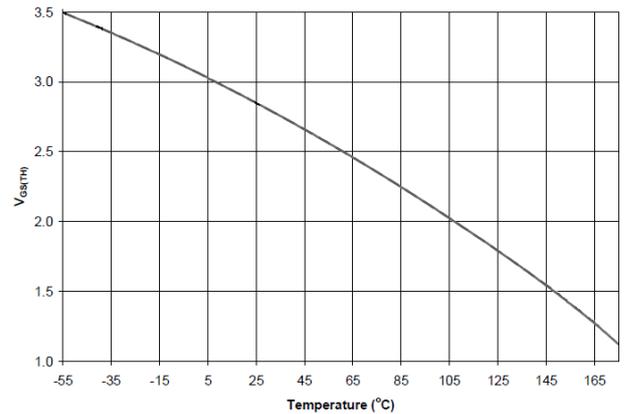


Figure.5 Threshold voltage comparison between simulation and experiment of 80V / 60 Power MOSFET.

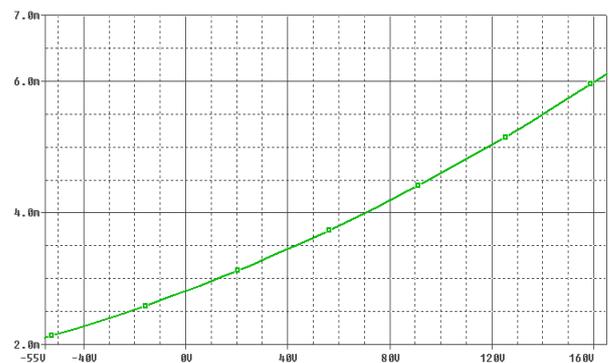
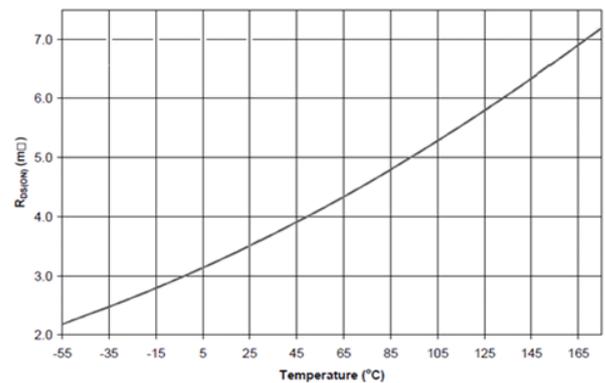


Figure 6. On-state resistance comparison between simulation and experiment of 80 V / 60 Power MOSFET.

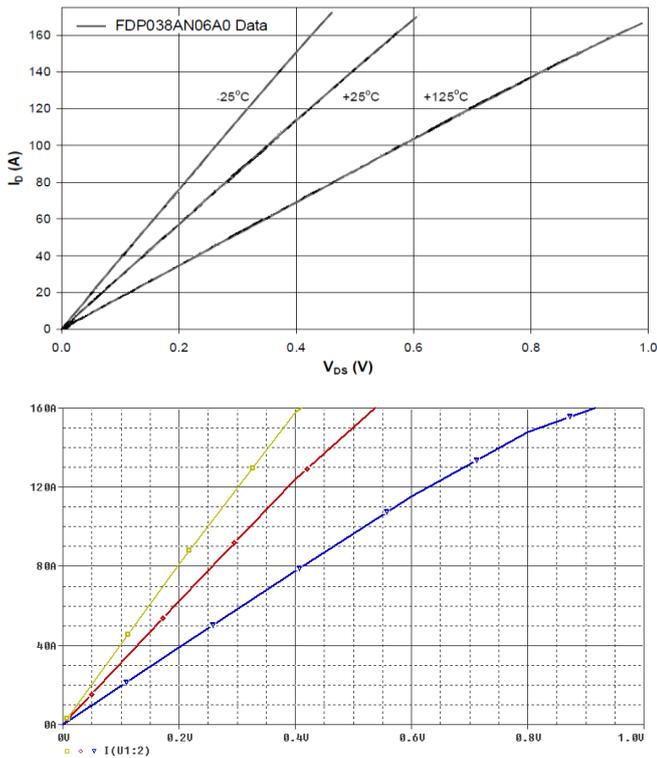


Figure 7. Forward characteristic comparison between simulation and experiment of 60 V / 80 MOSFET at (-25, +25, +125) °C.

IV. SIMULATING UNCLAMPED INDUCTIVE SWITCHING

The unclamped inductive switching (UIS) test circuit in Figure 5 was used to compare the performance of the VDMOSFET (3.5 mΩ, 60V, TO-263) self-heating MOSFET model with that of the standard model and measurement results.

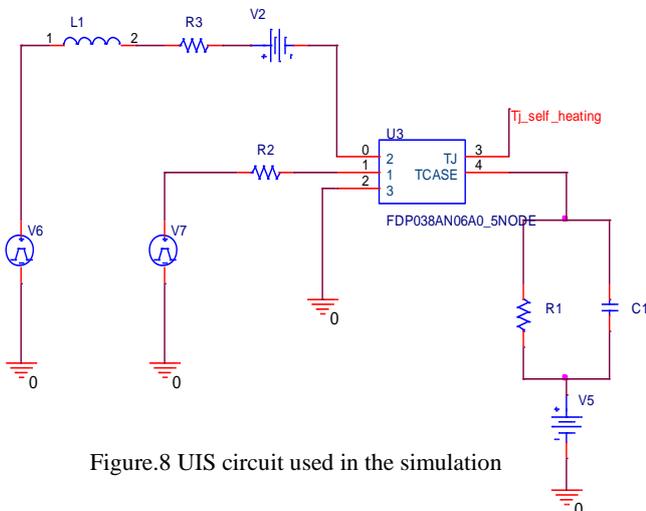


Figure.8 UIS circuit used in the simulation

The standard MOSFET model unclamped inductive switching simulation results were performed with PSPICE TNOM and .TEMP variables set to 25°C (Figure 6). The lack of temperature feedback to the model results in a drain-source breakdown voltage that is strictly drain current dependent.

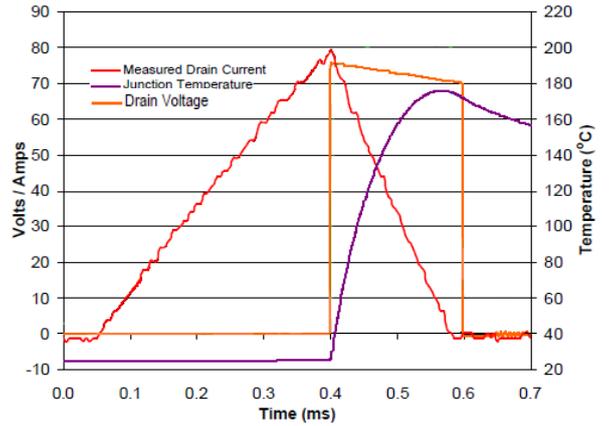


Figure.9 Measured UIS waveforms for a Power MOSFET standard model

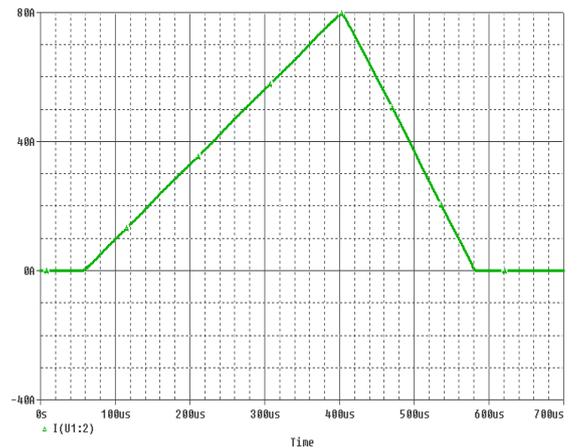


Figure 9.a Simulated drain current for the Power MOSFET transistor



Figure.9.b Simulated drain voltage for the Power MOSFET transistor without self heating effect

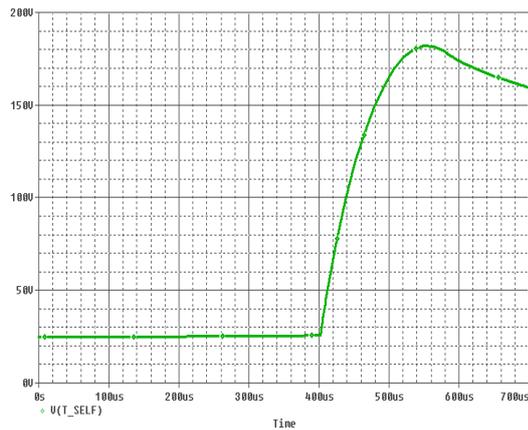


Figure.9.c Simulated Junction temperature for Power MOSFET transistor

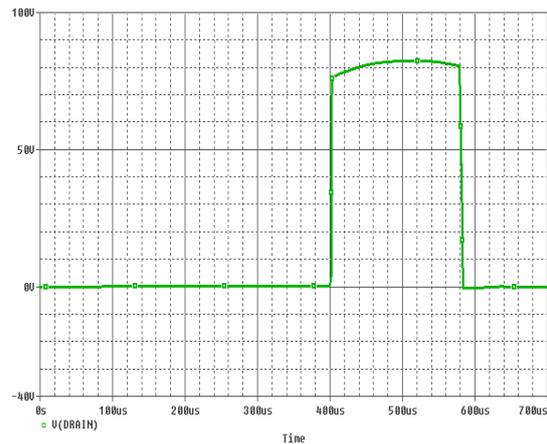


Figure.7.b Simulated drain Voltage for the Power MOSFET transistor with self heating effect

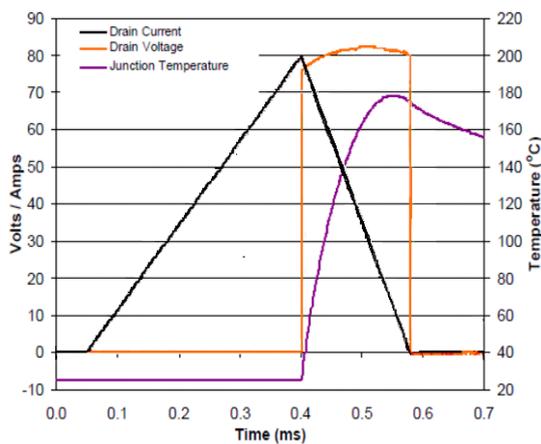


Figure.7 Measured UIS waveforms for a Power MOSFET Self-Heating Model

Unclamped inductive simulation results for a self heating MOSFET model are shown in Figure7. (a, b). Simulated drain-source breakdown voltage demonstrates the model dependence on junction temperature as well as drain current. Excellent agreement exists.

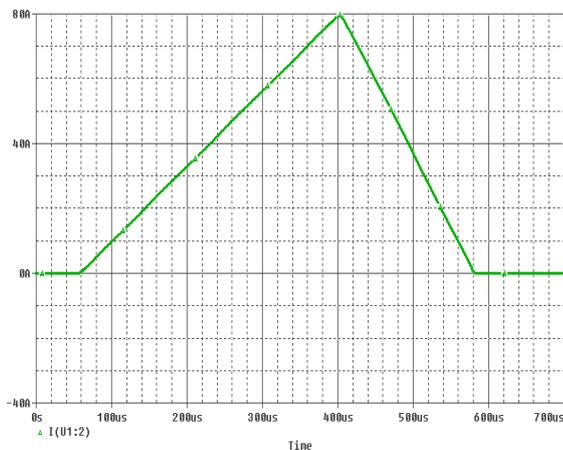


Figure.7.a Simulated drain current for the Power MOSFET transistor

V. FUTURE MODEL DEVELOPMENTS

Minor inaccuracy is introduced if previously published Fairchild Semiconductor MOSFET models are modified to become self-heating models, but are within device tolerance. The inaccuracy can be eliminated by including the variable $T_{ABS}=25$ in the level-1 NMOS MOSFET and the intrinsic body diode models during device specific model calibration, permitting full compatibility of the model with the new self-heating model. This term was included for the standard MOSFET model calibration of the Power MOSFET.

VI. CONCLUSION

In this paper, a 60 V / 80A power MOSFET has been tested and modeled. The static characteristics, such as the forward and transfer curves, the on-state resistance, and threshold voltage, have been extracted and calculated under different temperatures. The temperature dependency of them has also been analyzed. The comparison of static characteristic between Pspice model and measured data show good agreement with each other.

By modification of built-in SPICE-like electrical model, adding simple ladder network model of MOSFET's thermal behaviour, relatively simple and accurate electro-thermal model of power MOSFET is obtained. Such a model can be successfully used in most standard electrical circuit simulators for determining semiconductor's operating temperature during various operation cycles. Final verification was provided on the unclamped circuit simulation example, when over temperature reaction time was measured and simulated for the same conditions. Good agreement of measured and simulated results confirms the expectations.

REFERENCES

- [1] J. Wang, T. Zhao, J. Li, A. Q. Huang, R. Callanan, F. Husna, A. Agarwal, "Characterization, modeling, and application of 10-kV SiC MOSFET," *IEEE Transactions on Electron Devices*, vol. 55, no. 8, pp. 1798-1806, Aug. 2008.
- [2] S. Li, L. M. Tolbert, F. Wang, F. Z. Peng, "Reduction of stray inductance in power electronic modules using basic switching cells," *IEEE Energy Conversion Congress and Exposition (ECCE)*, 12-16 Sept. 2010,
- [3] F. Di Giovanni, G. Bazzano, A. Grimaldi, "A New PSPICE Power MOSFET Subcircuit with Associated Thermal Model", *PCIM 2008 Europe*, pp. 271-276.
- [4] C.F. Wheatley, Jr. and H.R. Ronan, Jr., "Switching Waveforms of the L 2 FET: A 5VOLT Gate Drive Power MOSFET,"
- [5] D. T. Zweidinger, S. G. Lee, R. M. Fox, "Compact Modeling of BJT Self-Heating in SPICE", *IEEE Transactions on Computer-Aided Design of IC and Systems*, Vol. 12 No. 9, pp.1368-1375, 2003.
- [6] A. Hefner, "Simulating the dynamic electrothermal behaviour of power electronic circuits and systems", *IEEE Transactions on Power Electronics*, Vol.8, No.4, Oct. 1993.
- [7] Szekely, V., Van Bien, T., "Fine Structure of Heat Flow Path in Semiconductor Devices: Measurement and Identification Method," *Solid-State Electronics*, Vol. 31 (2002), pp. 1363-1368.
- [8] C.F. Wheatley, Jr., H.R. Ronan, Jr., and G.M. Dolny, "Spicing-up SPICE II Software For Power MOSFET Modeling," Fairchild Semiconductor, Application Note AN7506, February 2006.
- [9] P. Nance, M. Marz, Thermal Modelling of Power Electronic System. *PCIM Europe, 2/2000*, pp. 20-27.
- [10] A. Maxim, D. Andreu, J. Boucher, "SPICE electrothermal modeling of power integrated circuits", *IEEE MIEL'97 Conference*.
- [11] Apendoorn, S. Schmitt, H.W. DE Donker, "An electrical model of a NPT-IGBT including transient temperature effects realized with PSPICE Device Equations modeling", *Proceeding of IEEE ISIE'97 Conference*, pp. 223-228.
- [12] Q. Chen, X. Yang, Z. Wang, L. Zhang, and M. Zheng, "Thermal design considerations for integrated power electronics modules based on temperature distribution cases study," in *IEEE PESC Rec.*, Orlando, FL, Jun. 17-21, 2007, pp. 1029-1035.

Lotfi messaadi was born in Algeria in 1985. He obtained his Engineer and his Magister degrees in Electronics in 2007 and 2010 respectively. He works now towards PhD degree in electronics. His research interests are on simulation and modeling of power devices. He is currently an assistant Lecturer, in electronic's Department, Batna University, Algeria.